What is claimed is:

- 1. A layout of a flash memory having symmetric select transistors, comprising:
- 5 a memory cell array;
 - a polysilicon gate extending in a direction perpendicular to the memory cell array with a plurality of pairs of sources/drains arranged at two sides thereof for forming a plurality of select transistors; and
- a wire connecting the plurality of select transistors and the memory cell array.
 - 2. The layout according to claim 1, wherein the wire comprises a segment parallel to the polysilicon gate.
 - 3. A layout of a flash memory having symmetric select transistors, comprising:
 - a memory cell array; and
 - a polysilicon gate corresponding to a plurality of select transistors extending in a direction perpendicular to the memory cell array;
 - wherein the plurality of select transistors are arranged substantially symmetric with respect to the memory cell array.

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4. The layout according to claim 3, further comprising a metal wire extending from the memory cell array toward the polysilicon gate for connecting the plurality of select transistors to a bit line of the memory cell array.

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